

12 Pages

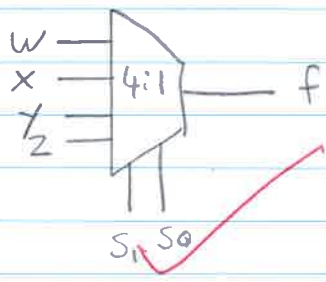
1. Please give the information requested in the boxes below
2. Enter your name in the space provided to the right, fold the paper over and seal down (using the label provided) to hide your name.
3. The answers must be legibly written. The Examiners can refuse to mark answers that are not legible. It is the responsibility of the candidate.
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5. Begin each answer on a fresh page. Do all rough work in the answer book and cross it through.
6. No part of this book is to be torn out; it must be handed in complete.
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1	Student Number	2112884
2	Title of Examination Paper	Electronics 2
3	Module Code	ACDA6001
4	Date and Time of Examination	10/05/2023 9am
5	Examination Venue	IQ310
6	Seat Number	042
7	Number of Answer Books handed in	

[illegible]

$\frac{73}{100}$

Q1) d)



2

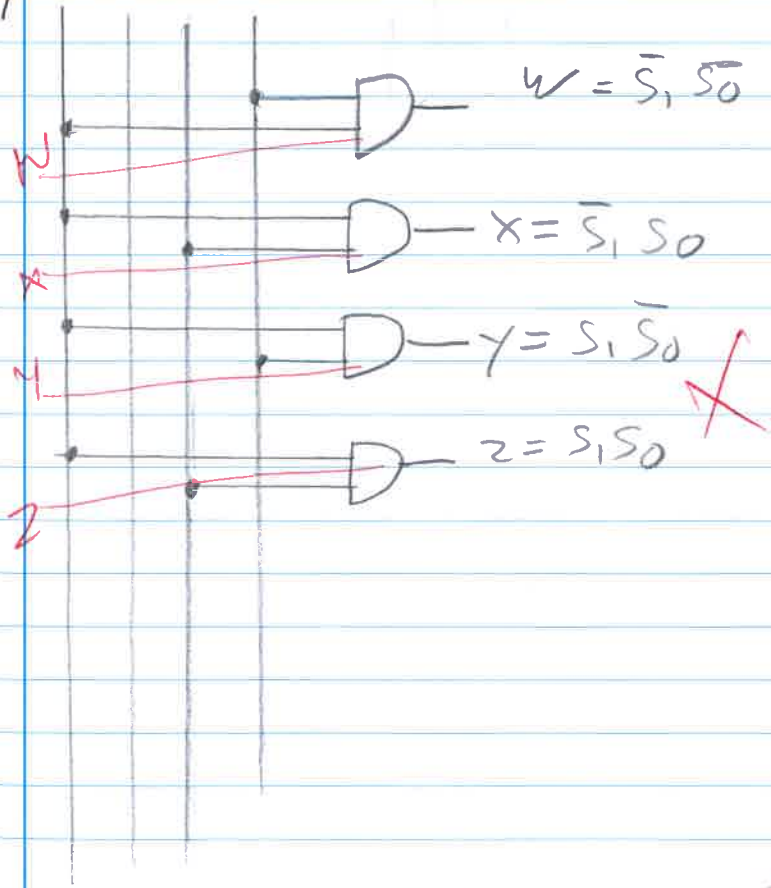
b)

Input				Selectors		Output
Z	Y	X	W	S ₁	S ₀	F
0	0	0	1	0	0	w
0	0	1	0	0	1	x
0	1	0	0	1	0	y
1	0	0	0	1	1	z

$F = \bar{S}_1 \bar{S}_0$

2

c) $S_1, \bar{S}_1, S_0, \bar{S}_0$



0

4

Q 1) ii)

```

use library IEEE;
use IEEE.STD-logic-1164.all;
use IEEE.STD-Logic-Arch.all;
use IEEE.STD-Logic-unsigned.all;

```

entity of Max4-1 is

```

port (w, x, y, z: in bit;
      S1, S0: in bit;
      F: out bit;
end Max4-1;

```

Architecture dataflow of Max4-1 is

```

begin
process (w, x, y, z, S1, S0);
begin
if S1='0' and S0='0' then
    F <= w;
elsif S1='0' and S0='1' then
    F <= x;
elsif S1='1' and S0='0' then
    F <= y;
else
    F <= z;
end if;
end process;
end dataflow;

```

1 ✓

4 ✓

5 ✓

$$\frac{14}{20}$$

10

Q1 = 14

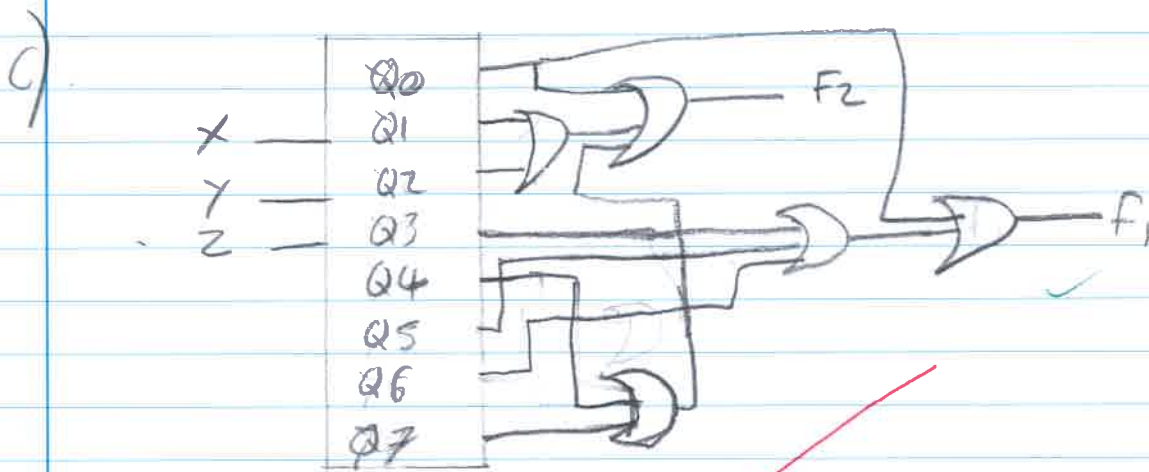
Q5 i) a)

	x, y, z	F ₁	F ₂
0	0 0 0	1	1
1	0 0 1	0	1
2	0 1 0	0	1
3	0 1 1	1	0
4	1 0 0	0	1
5	1 0 1	1	0
6	1 1 0	1	0
7	1 1 1	0	1

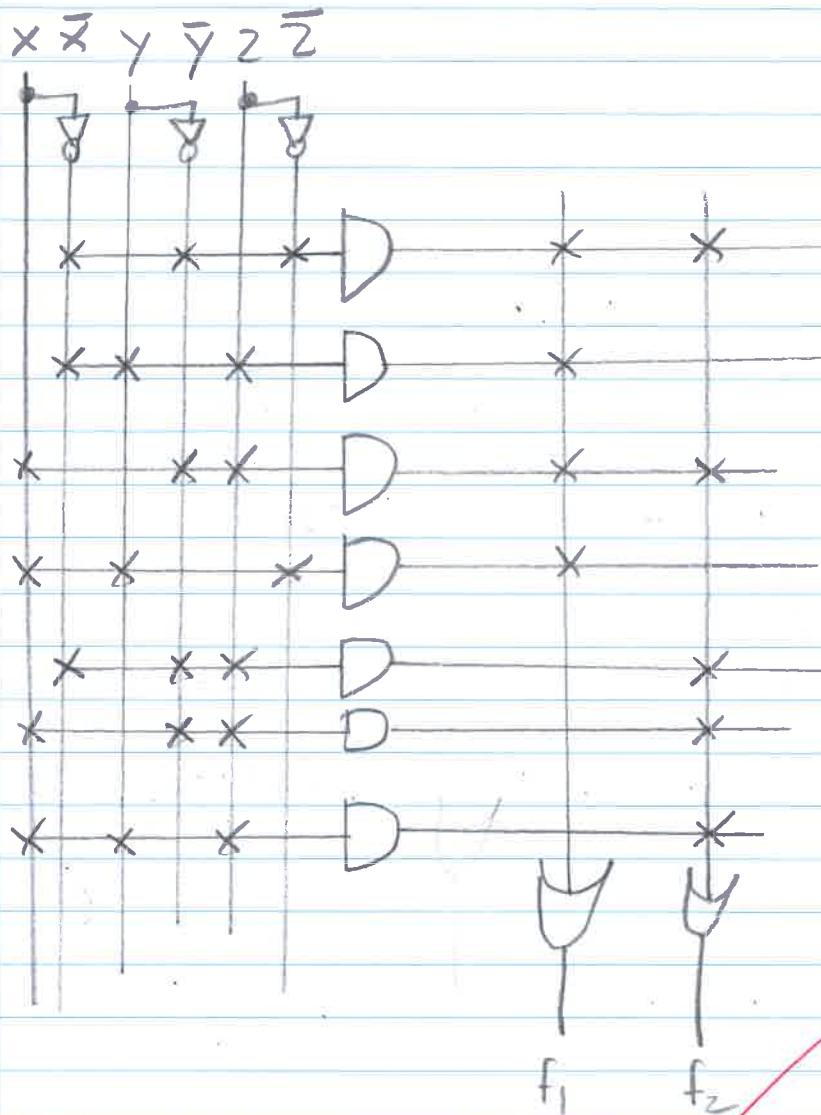
B)

$$F_1 = \bar{x}\bar{y}\bar{z} + \bar{x}yz + x\bar{y}z + xy\bar{z}$$

$$F_2 = \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + x\bar{y}\bar{z} + x\bar{y}z + xy\bar{z}$$



Q5d) $F_1 = \bar{x}\bar{y}\bar{z} + \bar{x}yz + x\bar{y}z + xy\bar{z}$
 $F_2 = \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + x\bar{y}\bar{z} + x\bar{y}z + xyz$



6

20
20

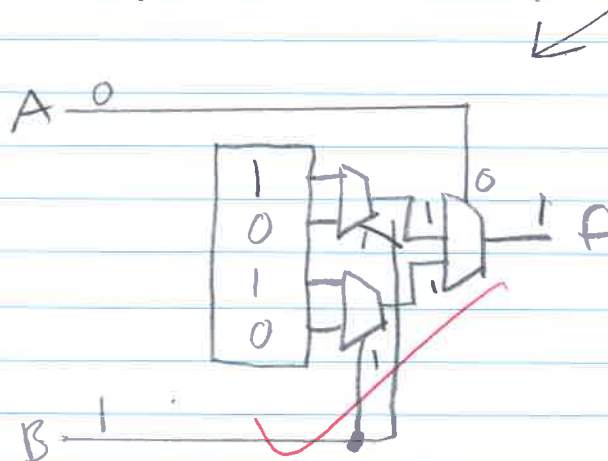
b

20
20

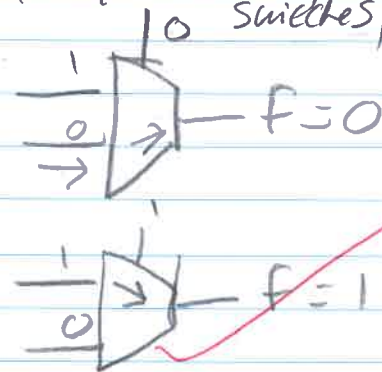
- Q6i) A LUT or look up table is the most common logic block. They can store bit data as either a 0 or 1. However, they are volatile, meaning they lose their value if powered off. LUT's are used in FPGAs to ~~store~~ store bit values. If they receive an input of 1 then the top

2

An example of a 2 input LUT is shown below:



(example on how LUT switches)



4

2

If A=0 and B=1 then f^{output} would be 1.

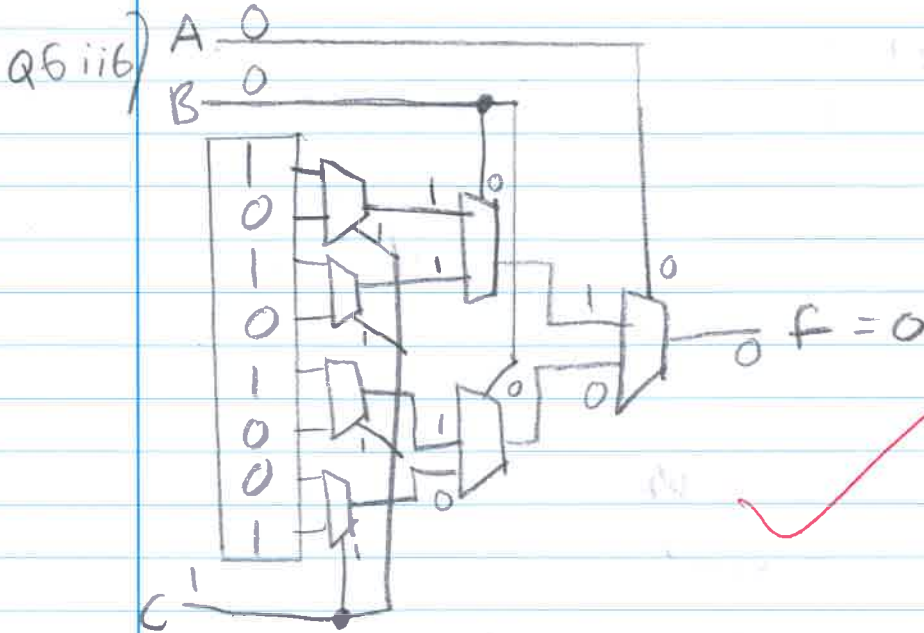
ii) $f = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

a)

	A	B	C	F
0	0	0	0	1
1	0	0	1	0
2	0	1	0	1
3	0	1	1	0
4	1	0	0	1
5	1	0	1	0
6	1	1	0	0
7	1	1	1	1

2

10



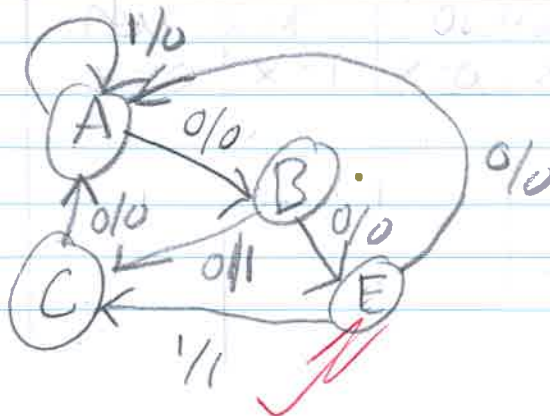
Q2i)

Present State	Next State		Output	
	$x=0$	$x=1$	$x=0$	$x=1$
A	B	D	0	0
B	E	C	0	1
C	D	C	0	0
D	B	D	0	0
E	A	C	0	1

reduced state table

Present State	Next State		Output	
	$x=0$	$x=1$	$x=0$	$x=1$
A	B	A	0	0
B	E	C	0	1
C	A	C	0	0
E	A	E	0	1

'D' replaced by 'A'



ia) $AC=00$
 $BC=01$
 $CC=10$
 $EC=11$

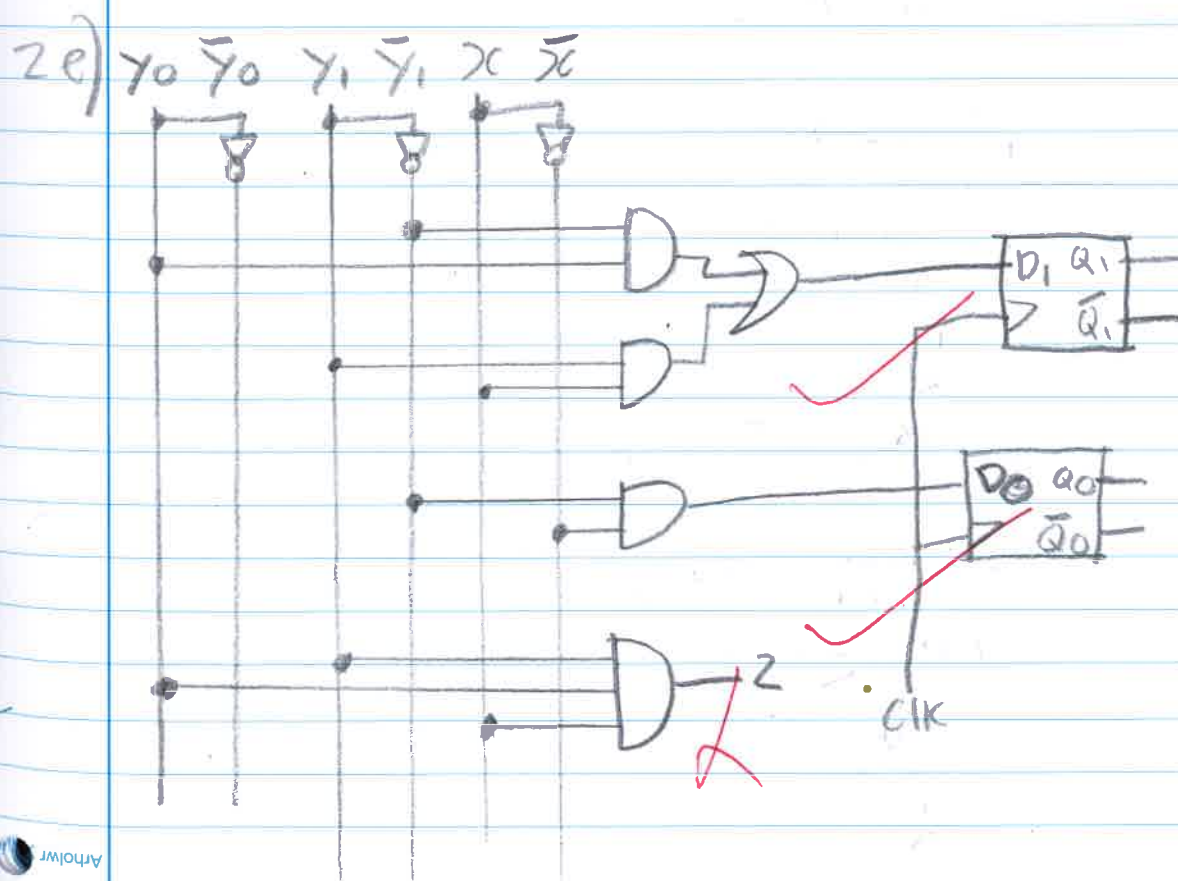
2c)

$$D_2 = \overline{y_1} \overline{x}$$

Y_1

	00	01	11	10
0	1	0	0	1
1	0	0	0	0

Y_1	Y_2	00	01	~~11~~	~~10~~
0		0	0	0	0
1		0	0	1	0



Q3)i) a) $B \times Q =$
 $-5 \times 4 = -20$

$B(-5) = 1100$
 $-B(5) = 0101$
 $Q = 0100$

$S = 0101$

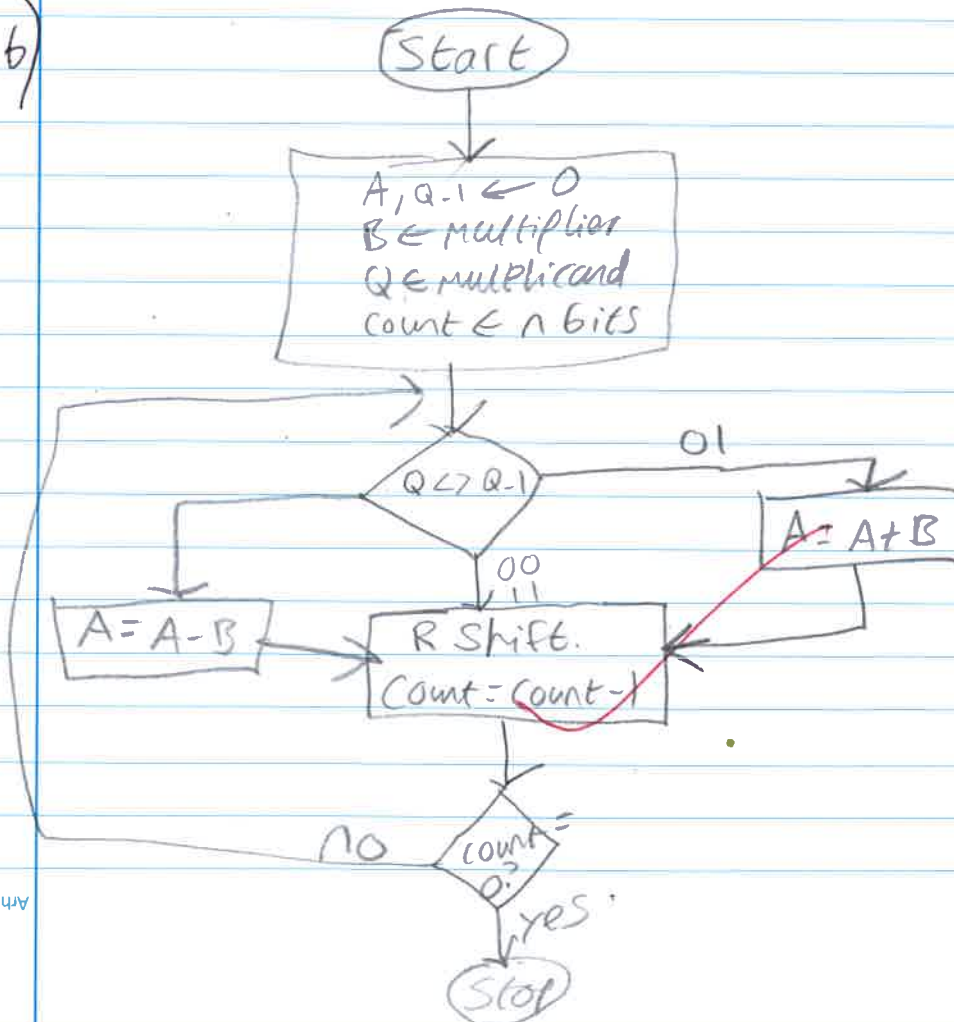
$1011 + 1$
 1100

0101
 $1011 +$
 1100

1 indicates negative.

$$\begin{array}{r} 0100 \times \\ 1100 \\ \hline 00000000 \\ 00000000 \\ 11110000 \\ 11100000 \\ \hline 11101000 = -20 \end{array}$$

Q3b)



30) $-B(5) = 0101$ $-20 = 11101000$
 $B(-5) = 1100$
 $Q(4) = 0100$

Step	A	Q	Q ₋₁	Process
0	0000	0100	0	Initial ✓
1	0000	0010	0	Rshift ✓
2	0000	0001	0	Rshift?
3	0101	0001	0	Rshift?
4	0010	1000	1	A = A + B
	1110	1000	1	Rshift.

$A + Q = -20$

2

06
20

Step 3) $A = A - B = A + (-B) =$

$$\begin{array}{r} 0000+ \\ 0101 \\ \hline 0101 \end{array}$$

2

Step 4) $A + B =$

$$\begin{array}{r} 0000+ \\ 1100 \\ \hline 1100 \end{array}$$

Q₃ = 10Q₃ = 10

3ii) library IEEE;
 use ~~IEEE~~ IEEE.STD-logic-1164.all;
 use IEEE.STD-Logic-Arith.all;
 use IEEE.STD-Logic-unsigned.all;

entity of Multiply is
 port(A, B: in bit_vector(1 downto 0);
 P: out bit_vector(3 downto 0);
 end Multiply;

Architecture of Multiply is
 begin

A₁ A₀
 B₁ B₀
 B₀ A₁
 B₀ A₀

P(0) <= (A(0) and B(0));
 P(1) <= (A(0) and B(1)) xor (A(1) and B(0));
 P(2) <= (A(1) and B(0)) xor (A(0) and B(1)) xor (A(1) and B(1));
 P(3) <= (A(1) and B(0)) xor (A(0) and B(1)) and (A(1) and B(1));
 end data;

04
 20